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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|----------------|------------------------------|---------------------|------------------|
| 10/597,089 | 07/11/2006 | Rick Franciscus Jozef Stopel | NL040072 | 5865 |
| 65913 NXP, B.V. | 7590 03/17/200 | EXAMINER | | |
| NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131 | | | TABLER, MATTHEW C | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2819 | |
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| | | | NOTIFICATION DATE | DELIVERY MODE |
| | | | 03/17/2009 | ELECTRONIC |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| | Application No. | Applicant(s) | | | | |
|---|---|--|--|--|--|--|
| | 10/597,089 | STOPEL ET AL. | | | | |
| Office Action Summary | Examiner | Art Unit | | | | |
| | MATTHEW C. TABLER | 2819 | | | | |
| The MAILING DATE of this communication app | ears on the cover sheet with the c | orrespondence address | | | | |
| Period for Reply | | | | | | |
| A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA. - Extensions of time may be available under the provisions of 37 CFR 1.1: after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period v. Failure to reply within the set or extended period for reply will, by statute. Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). | ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE | N. nely filed the mailing date of this communication. D (35 U.S.C. § 133). | | | | |
| Status | | | | | | |
| 1)⊠ Responsive to communication(s) filed on 11 Ju | ılv 2006 | | | | | |
| | action is non-final. | | | | | |
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| closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. | | | | | | |
| Disposition of Claims | | | | | | |
| 4)⊠ Claim(s) <u>1-16</u> is/are pending in the application. | | | | | | |
| 4a) Of the above claim(s) is/are withdrawn from consideration. | | | | | | |
| 5) Claim(s) is/are allowed. | | | | | | |
| 6)⊠ Claim(s) <u>1-8 and 10-16</u> is/are rejected. | | | | | | |
| 7)⊠ Claim(s) <u>9</u> is/are objected to. | | | | | | |
| 8) Claim(s) are subject to restriction and/o | r election requirement. | | | | | |
| Application Papers | | | | | | |
| 9)☐ The specification is objected to by the Examine | r. | | | | | |
| 10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner. | | | | | | |
| Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). | | | | | | |
| Replacement drawing sheet(s) including the correct | ion is required if the drawing(s) is obj | ected to. See 37 CFR 1.121(d). | | | | |
| 11)☐ The oath or declaration is objected to by the Ex | aminer. Note the attached Office | Action or form PTO-152. | | | | |
| Priority under 35 U.S.C. § 119 | | | | | | |
| 12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of: | | | | | | |
| a)⊠ All b)⊡ Some c)⊡ None of a superiority documents have been received. | | | | | | |
| 2. Certified copies of the priority documents have been received in Application No | | | | | | |
| 3. Copies of the certified copies of the priority documents have been received in this National Stage | | | | | | |
| application from the International Bureau (PCT Rule 17.2(a)). | | | | | | |
| * See the attached detailed Office action for a list of the certified copies not received. | | | | | | |
| | | | | | | |
| Attachment(s) | | | | | | |
| 1) Notice of References Cited (PTO-892) | 4) Interview Summary | | | | | |
| 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) | Paper No(s)/Mail Da 5) Notice of Informal P | | | | | |
| Paper No(s)/Mail Date | 6) Other: | •• | | | | |

DETAILED ACTION

This office action is in response to application 10/597,089 filed on July 11th, 2006. Currently, claims 1-16 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5-8, and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (US Patent 6,424,585) patented on July 23rd, 2002.

Regarding claim 1, Ooishi shows a pull-up circuit (Figure 8), comprising an operational amplifier (3), having a reference voltage input (Vref) connected to a first input thereof (inverting input), and a first transistor (2), controlled by the output of the operational amplifier (6), the first transistor having a first terminal connected to a first supply voltage input (VCE) and having a second terminal connected to a pull-up circuit output (5) and to a second input of the operational amplifier (non-inverting input), such that, when the operational amplifier (3) is enabled, it acts to bring the voltage on the pull-up circuit output equal to the voltage on the reference voltage input (voltage at output node 5 matches Vref when amplifier is enabled).

Regarding claim 5, Ooishi shows a second transistor (PT), having its conducting path connected between the first supply voltage input (VCE) and the output of the

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operational amplifier (6), controlled such that it is turned off while the operational amplifier is enabled (OFF when amplifier enabled).

Regarding claim 6, Ooishi shows the second transistor is a PMOS transistor (PT is PMOS).

Regarding claim 7, Ooishi shows a pull-up resistance (shown in alternative embodiment in Figure 29), switchably connected between a second supply voltage input (gate voltage of N35) and the pull-up circuit output (5), and logic circuitry (transistor N35), for determining whether a voltage on the second supply voltage input (gate) is greater than a threshold voltage (open/close threshold of transistor N35) and, when it is determined that the voltage on the second supply voltage input is greater than the threshold voltage (gate voltage > threshold voltage; logic 1 applied to N35), for disabling the operational amplifier (amplifier disabled from node 5 and load 7) and for connecting the pull-up resistance (N35 is ON) between the second supply voltage input (gate voltage) and the pull-up circuit output (5), and when it is determined that the voltage on the second supply voltage input is not greater than the threshold voltage (gate voltage < threshold voltage, logic 0 applied to N35), for enabling the operational amplifier (amplifier enabled at node 5 and to load 7) and for disconnecting the pull-up resistance (N35 is OFF).

Regarding claim 8, Ooishi shows the pull-up resistance is switchably connected between a regulated voltage (VCE) obtained from the second supply voltage input (gate voltage) and the pull-up circuit output (5).

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Regarding claim 10, Ooishi shows a USB transceiver, comprising a pull-up circuit as claimed in claim 1, wherein the first terminal is connectable to a USB bus voltage. (Intended Use: It has been held that a recitation directed to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).)

Regarding claim 11, Ooishi shows a USB transceiver, for use in a USB Device, the USB transceiver comprising a pull-up circuit as claimed in claim 7, wherein the first terminal is connectable to a USB bus voltage, and wherein the second supply voltage input of the pull-up circuit is connectable to a power supply of the USB Device.

(Intended Use: It has been held that a recitation directed to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).)

Regarding claim 12, Ooishi shows a USB transceiver, as claimed in claim 11, further comprising a DC-DC converter, for forming a regulated voltage from the power supply of the USB Device, wherein the pull-up resistance is switchably connected between the regulated voltage and the pull- up circuit output. (Intended Use: It has been held that a recitation directed to the manner in which a *claimed apparatus is intended to be employed* does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).)

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Regarding claim 13, Ooishi shows a USB transceiver as claimed in claim 10, comprising a first pull-up circuit having its pull-up circuit output connected to a D+ line of a USB Device, and a second pull-up circuit having its pull-up circuit output connected to a D- line of a USB Device. (Intended Use: It has been held that a recitation directed to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).)

Regarding claim 14, Ooishi shows a transceiver as claimed in claim 10, suitable for use in a USB on-the-go device. (<u>Intended Use:</u> It has been held that a recitation directed to the manner in which a *claimed apparatus is intended to be employed* does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).)

Regarding claim 15, Ooishi shows a USB device, comprising a USB transceiver as claimed in claim 10. (Intended Use: It has been held that a recitation directed to the manner in which a *claimed apparatus is intended to be employed* does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).)

Regarding claim 16, Ooishi shows a USB on-the-go device, comprising a USB transceiver as claimed in claim 10. (<u>Intended Use:</u> It has been held that a recitation directed to the manner in which a *claimed apparatus is intended to be employed* does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi in view of design choice case law.

Regarding claim 2, Ooishi discloses the claimed invention expect for a plurality of diodes, connected in series between the first supply voltage input and ground, with the reference voltage input connected at an intermediate point in said series connection of diodes (Figure 133 shows reference voltage generator coupled between VCE and GND).

It would have been an obvious matter of design choice to use a voltage divider with diodes to provide a reference voltage and since applicant has not disclosed that a voltage divider with diodes solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with any commonly used circuit component that generates a stable, reference voltage.

Regarding claim 3, Ooishi discloses the claimed invention expect for the first input of the operational amplifier is the non-inverting input, and the second input of the operational amplifier is the inverting input.

It would have been an obvious matter of design choice to choose to use these inputs and since applicant has not disclosed that these inputs solve any stated problem or are for any particular purpose, it appears that the invention would perform equally well by flipping the inputs of the amplifier and replacing the output n-type transistor with an output p-type transistor.

Regarding claim 4, Ooishi discloses the claimed invention expect for an NMOS transistor.

It would have been an obvious matter of design choice to use an n-type output transistor and since applicant has not disclosed that an n-type transistor solves any stated problem or is for any particular purpose, it appears that the invention would perform equally well with a p-type output transistor receiving an inverted result (done by flipping inputs to amplifier).

Allowable Subject Matter

Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claim 9 claims the pull-up resistance comprises "first and second resistors connected in parallel between the second supply voltage input and the pull-up circuit output when the pull-up circuit is in idle mode, and wherein one of said resistors is

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deactivated to thereby increase the pull-up resistance when the pull-up circuit is in active mode."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW C. TABLER whose telephone number is (571)270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. C. T./
Examiner, Art Unit 2819
March 16, 2009
/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2819